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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,552	12/05/2003	Ian Rippke	42339-198344	7984

26694 7590 09/06/2005

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,552	RIPPKE ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14,26-33,35,36 and 38-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13* is/are allowed.

6)☒ Claim(s) *1-5,7,8,26-33,35,36 and 38-41* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/12/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26-29, 31 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata et al (US 6,876,055 B2).

Regarding claim 26, Iwata et al. discloses in figure 17 a device comprising a layer 314 of a first conductivity type (col. 22, line 14) formed directly on a semiconductor substrate 312; a first transistor 328 (col. 23, line 54) disposed in the layer 314; a body contact 321 (col. 22, lines 31-32) disposed in the layer; and a resistance region 316 (col. 2, line 10) disposed in the layer between the first transistor and the body contact region, the resistance region having a resistivity higher than a resistivity of the layer, wherein the substrate is of said first conductivity type (col. 2, line 8).

Element 312 as shown in figure 17 is the layer on which the semiconductor device is formed. Therefore, element 312 can function as a substrate.

Regarding claim 27, Iwata et al. discloses in figure 17 the resistance region 316 substantially isolates the first transistor 328 from the body contact region 321.

Regarding claim 28, Iwata et al. discloses in figure 17 a second transistor 325 (col. 23, line 53) disposed in the layer, wherein the second transistor is disposed on a same side of the resistance region as the body contact region 321.

Regarding claim 29, Iwata et al. discloses in figure 17 the body contact region 321 is adapted to be coupled to ground. Note that the body contact region 321 is coupled to bias input 329 (col. 22, line 29), which is considered "ground" herein.

Regarding claim 31, Iwata et al. discloses the resistance region 316 has an impurity concentration lower than an impurity concentration of the layer (see rejection of claim 6 above).

Regarding claim 33, Iwata et al. discloses in figure 17 the resistance region 316 occupies substantially an entire cross sectional area of the layer between the first transistor 328 and the body contact region 321.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8 and 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. in view of Wakamiya et al. (US 3,871,007).

Regarding claim 1, similar to claim 26, Iwata et al. discloses in figure 10 substantially all the structures set forth in the claimed invention except the resistance having a non-zero impurity concentration lower than an impurity concentration of the layer. However, Wakamiya et al. discloses in figure 2F the resistance 204 (col. 3, lines 35-37) having a non-zero impurity concentration lower than an impurity concentration of the layer 203 (see figure 3, which shows the impurity concentration of the single crystal layer 203 (line 302) is possibly higher than that of the polycrystalline layer 204 (line 301) that functions as resistance). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Iwata et al. by having the resistance having a non-zero impurity concentration lower than an impurity concentration of the layer to provide an integrated circuit of excellent high speed characteristics (col. 4, lines 36-37, Wakamiya et al.).

Regarding claim 2, Iwata et al. discloses in figure 10 a second transistor 326 (col. 21, line 60) disposed in the layer, wherein the second transistor is disposed on a same side of the resistance region 333 as the body contact region 322.

Regarding claim 3, Iwata et al. discloses the first conductivity type is a p type (col. 21, line 44). The phrase "body contact region is adapted to be coupled to ground" is merely the intended use. Further, since applicant does not

specifically define the structure and voltage level of ground, the well bias input 331 is considered "ground".

Regarding claim 4, Iwata discloses in figure 10 the body contact region 330 is coupled to a power supply. Further, it is well known in the art that n type and p type can be interchanged, merely depending upon certain application and design.

Regarding claim 5, Iwata discloses in figure 10 a substrate 311 (col. 21, line 43), the layer 315 being disposed on top of the substrate.

Regarding claim 8, Iwata et al. discloses in figure 10 the resistance region 333 occupies substantially an entire cross sectional area of the layer 315 between the first transistor 327 and the body contact region 330.

Regarding claim 38, Iwate et al. discloses in figure 10 a device comprising a layer of a first conductivity type 315 (col.21, line 44); a first transistor 327 disposed in the layer (col. 21, line 51); a body contact region 322 disposed in the layer; a second transistor 326 disposed in the layer, wherein the second transistor is disposed on a same side of the resistance region as the body contact region; and a resistance region 333 disposed in the layer between the first transistor 327 and the body contact region, the resistance region having a resistivity higher than a resistivity of the layer, wherein the resistance region has an impurity concentration lower than an impurity concentration of the layer (see rejection of claim 6 above). Iwata et al. does not disclose the resistance having a non-zero impurity concentration lower than an impurity concentration of the layer. However, Wakamiya et al. discloses in figure 2F the resistance 204 (col. 3, lines

35-37) having a non-zero impurity concentration lower than an impurity concentration of the layer 203 (see rejection of claim 1 above). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Iwata et al. by having the resistance having a non-zero impurity concentration lower than an impurity concentration of the layer to provide an integrated circuit of excellent high speed characteristics (col. 4, lines 36-37, Wakamiya et al.).

Regarding claim 39, Iwata et al. discloses in figure 10 a substrate 311, the layer 315 being disposed on top of the substrate.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. in view of Yamaguchi et al. (US 6,867,106 B2)

Regarding claim 32, Iwata et al. discloses in figure 10 substantially all the structure set forth in the claimed invention except a discrete capacitor coupled between a body and a source of the first transistor. However, Yamaguchi et al. discloses on figure 3 a discrete capacitor coupled between a body and a source of the first transistor (col. 8, lines 21-26). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Iwata et al. by having a discrete capacitor coupled between a body and a source of the first transistor to suppress performance deterioration of the transistors (col. 3, lines 16-17 of Yamaguchi et al.).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. and Wakamiya et al. in view of Yamaguchi et al.

Regarding claim 7, Iwata et al. and Wakamiya et al. disclose substantially all the structure set forth in the claimed invention except a discrete capacitor coupled between a body and a source of the first transistor. However, Yamaguchi et al. discloses on figure 3 a discrete capacitor coupled between a body and a source of the first transistor (col. 8, lines 21-26). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Iwata et al. and Wakamiya et al. by having a discrete capacitor coupled between a body and a source of the first transistor to suppress performance deterioration of the transistors (col. 3, lines 16-17 of Yamaguchi et al.).

Claims 30, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. in view of Wong et al. (US 6,246,094 B1).

Regarding claims 30, 35 and 36, Iwata et al. discloses on figure 10 substantially all the structure set forth in the claimed invention except the layer being epitaxial layer. However, Wong et al. discloses on figure 2D the layer 14 being epitaxial layer (col. 4, line 67 and col. 5, line 1). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Iwata et al. by having the layer being epitaxial layer to prevent latch up in a CMOS integrated circuit (col. 1, lines 10-12).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. and Wong et al. in view of Wakamiya et al.

Regarding claim 41, Iwata et al. and Wong et al. substantially all the structures set forth in the claimed invention except the resistance having a non-zero impurity concentration lower than an impurity concentration of the layer. However, Wakamiya et al. discloses in figure 2F the resistance 204 having a non-zero impurity concentration lower than an impurity concentration of the layer 203(see rejection of claim 1 above). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Iwata et al. and Wong et al. by having the resistance having a non-zero impurity concentration lower than an impurity concentration of the layer to provide an integrated circuit of excellent high speed characteristics (col. 4, lines 36-37, Wakamiya et al.).

Claims 14 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. and Wakamiya et al. in view of Wong et al.

Regarding claims 14 and 40, Iwata et al. and Wakamiya et al. disclose substantially all the structure set forth in the claimed invention except the layer being epitaxial layer. However, Wong et al. discloses on figure 2D the layer 14 being epitaxial layer (col. 4, line 67 and col. 5, line 1). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Iwata et al. and Wakamiya et al. by having the layer being epitaxial layer to prevent latch up in a CMOS integrated circuit (col. 1, lines 10-12).

Allowable Subject Matter

Claims 9-13 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The reference (s) of record do not teach or suggest, either singularly or in combination at least the limitation of "a resistance region disposed in the layer between the first transistor and the body contact region to substantially electrically isolate the first transistor from the body contact region, the resistance region having a resistivity higher than a resistivity of the layer; a second transistor coupled in series with the first transistor and having a control electrode adapted to receive an input signal of the device, the first transistor having a control electrode adapted to receive a bias voltage, and the body contact region being adapted to be coupled to a first one of power supply voltage and ground; and a load having a first end coupled to the first transistor and a second end adapted to be coupled to a second one of the power supply voltage and ground, a body of the second transistor being adapted to be coupled to the first one of the power supply voltage ground" for claim 9.

Response to Arguments

Applicant's arguments filed on 06/08/2005 have been fully considered but they are not persuasive.

With respect to claim 26, applicant argues that region 316 in figure 17 of Iwata is not disposed in a layer of a first conductivity type as claimed. However, region 316 is disposed in layer 324 of a first conductivity type. Note that region

316 is formed in and through layer 314 and reaches layer 312. Therefore, region 316 is.formed in layer 324. Further, applicant argues that if there is no p type substrate formed under the deep well region in figure 17 of Iwata, the device will not function properly. Therefore, layer 312 is a deep well region, not a substrate. However, "substrate" is a broad term. Since the claimed substrate contains no specific type of conductivity or structure that can be distinct from layer 312, layer 312 can function as a substrate along with layer 311, which is still part of the device.

Moreover, with respect to claims 30, 35 and 36, applicant argues that Wong et al. does not teach the use of an epitaxial layer is to prevent latch up. However, a semiconductor device as shown in figure 2D of Wong et al. is formed to prevent latch up and an epitaxial layer is a component of the device. Therefore, an epitaixal layer can help prevent latch up accordingly.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
August 30, 2005.

TOM THOMAS
SUPERVISORY PATENT EXAMINER